CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently amended) A transceiver for processing high data rate serial data, comprising:

a first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data;

a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data;

wherein the transceiver provides the first recovered clock, the second recovered clock, a reference clock, the first serial data and the second serial data to a plurality of clock based functionalities of the transceiver; and

wherein ~~the~~ each of the plurality of clock based functionalities performs processing of one of the first serial data and the second serial data in accordance with a clock chosen from ~~chooses~~ among the first recovered clock, the second recovered clock and the reference clock ~~for subsequent processing of one of the first serial data and the second serial data~~.

2. (Canceled)

3. (Currently amended) The transceiver of claim 1 ~~further comprising~~ wherein said second clock data recovery circuitry comprises a delay locked loop circuitry for receiving said second serial data and produces [[a]] said second recovered clock from the second serial data, wherein the transceiver provides the second serial data to the plurality of clock based functionalities and wherein each of the plurality of clock based functionalities uses one of the first recovered clock, the second recovered clock and the reference clock for ~~subsequent~~ processing of one of the first and second serial data.

4. (Currently amended) The transceiver of claim 1 wherein the first serial data is [[an]] a receive serial bit stream.

5. (Previously presented) The transceiver of claim 1 wherein the plurality of clock based functionalities comprises a portion of a programmable logic fabric.

6. (Currently amended) A transceiver for processing high data rate serial data, comprising:

a first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data, wherein the first circuitry provides the first recovered clock to a logic fabric comprising a first clock based functionality, a second clock based functionality, and a third clock based functionality; ~~and~~

a second circuitry for generating and providing a reference clock to the logic fabric;

a third circuitry for receiving second serial data and recovering a second recovered clock based on the second serial data, wherein the third circuitry provides the second recovered clock to the logic fabric; and

wherein each of the first, second and third clock based functionalities concurrently ~~perform~~ performs processing functions on one of the first serial data and the second serial data in accordance with a clock chosen from ~~by choosing~~ among the first recovered clock, the second recovered clock, and the reference clock.

7. (Canceled)

8. (Currently amended) A transceiver comprising:

a circuitry for receiving a plurality of input serial data streams;

a clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams;

a circuitry for providing a reference clock; and

a logic for selecting from the plurality of input serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block;

wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block in accordance with a clock chosen from ~~by choosing from~~ among the plurality of recovered clocks and said reference clock.

9. (Previously presented) The transceiver of claim 8 wherein the outgoing transmit block is one of a programmable transmit physical media attachment (PMA) module and a transmitter port.

10. (Currently amended) An integrated circuit, comprising:

at least one clock recovery circuitry coupled to receive a high data rate input data stream, wherein the at least one clock recovery circuitry recovers a plurality of recovered clocks based on the high data rate input data stream; and

a programmable logic fabric portion comprising a plurality of clock based functionalities, wherein each of the clock based functionalities performs ~~subsequent~~ processing on the high data rate input data stream in accordance with a clock chosen from ~~by choosing~~ among the plurality of recovered clocks and a reference clock.

11. (Previously presented) The integrated circuit of claim 10 wherein the high data rate input data stream is received according to a first protocol and is converted to a second protocol by the programmable logic fabric portion based on one of said plurality of recovered clocks.

12. (Currently amended) The integrated circuit of claim 11 further comprising a transmit circuitry coupled to receive the converted high data rate input data stream in the second protocol, wherein the programmable logic fabric portion provides the converted high data rate input data stream in the second protocol based on one of said plurality of recovered clocks.

13. (Previously presented) The integrated circuit of claim 11 wherein said at least one clock recovery circuitry comprises a second clock recovery circuit for recovering a second recovered clock based on an I/O serial data stream.

14. (Currently amended) A method of processing high data rate serial data, comprising:

receiving a high data rate input data stream;

recovering a first recovered clock based on the high data rate input data stream;

recovering a second recovered clock based on a transmitter clock;

providing the first and second recovered clocks to a programmable logic fabric portion comprising a plurality of clock based functionalities; and

performing ~~subsequent~~ processing of the high data rate input data stream in each of the plurality of clock based functionalities in accordance with a clock chosen from ~~by choosing~~ among the recovered clocks, wherein the high data rate input data stream is received according to a first protocol.

15. (Canceled)

16. (Currently amended) The method of claim [[15]] 14 wherein the high data rate input data stream is converted to a second protocol based on the first recovered clock.

17. (Canceled)

18. (Previously presented) The method of claim 16 further comprising transmitting the converted high data rate input data stream in the second protocol based on the second recovered clock.

19. (Currently amended) A method of processing high data rate serial data, comprising:

receiving a first serial bit stream and recovering a first recovered clock from the first serial bit stream;

receiving a second serial bit stream and recovering a second recovered clock from the second serial bit stream;

providing the first and second recovered clocks and a reference clock to a plurality of clock based functionalities; and

within each of the plurality of clock based functionalities, choosing among the first and second recovered clocks and the reference clock for ~~subsequent~~ processing of one of the first serial bit stream and the second serial bit stream by each of the plurality of clock based functionalities.

20. (Currently amended) The method of claim 19 wherein the first serial bit stream is [[an]] a receive serial bit stream.

21. (Previously presented) The method of claim 19 wherein the second serial bit stream is a transmit serial bit stream.

22. (Currently amended) A method of clock management in a processing block, comprising:

receiving a first data stream and recovering a first clock based on the first data stream;

providing the first clock to a logic fabric comprising a plurality of clock based functionalities;

receiving a second data stream and recovering a second clock based on the second data stream;

providing the second clock to the logic fabric;

providing a reference clock to the logic fabric; and

concurrently performing processing functions on one of the first data stream and the second data stream in the processing block by choosing, by each of the plurality of clock based functionalities, a clock from among the first and second clocks and the reference clock.

23. (Currently amended) A method for receiving and transmitting data, comprising:

receiving a plurality of input data streams;

recovering a corresponding plurality of clocks based on the plurality of input data streams;

determining at least one output port for providing outgoing data streams; and

providing each input data stream of the plurality of input data streams to the at least one output port ~~by choosing~~ in accordance with a clock chosen from among the plurality of recovered clocks;

wherein the at least one output port comprises a number of output ports that corresponds to a number of input data streams of the plurality of input data streams, and wherein the method further comprises determining, for each input data stream of the plurality of input data streams, an output port and providing each input data stream of the plurality of input data streams to the determined output ports based upon a chosen one of the plurality of recovered clocks.

24. (Canceled)